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TITLE: Multilayered structure for semiconductor device  
e.g. insulated gate  
bipolar transistor - includes barrier layer which is  
interposed between pure  
aluminium electrode and insulating film

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APPLICATION-DATA:

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INT-CL\_(IPC): H01L021/60; H01L029/43 ; H01L029/78

ABSTRACTED-PUB-NO: JP 11284176A

BASIC-ABSTRACT: NOVELTY - Insulating film (12) is formed over the n- layer (1), p layer (2) and a n+ layer (3). A pure aluminum electrode performs ohmic contact with the p and n+ layers through a wire (30). A gate electrode (11) is formed on the upper surface of a gate oxide film (10). A barrier layer (21) containing molybdenum silicide is provided between the electrode and insulating film.

USE - For semiconductor device e.g. power MOSFET, insulated gate bipolar transistor.

## \* NOTICES \*

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1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. \*\*\*\* shows the word which can not be translated.
3. In the drawings, any words are not translated.

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DETAILED DESCRIPTION

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## [Detailed Description of the Invention]

[0001]

[The technical field to which invention belongs] this invention relates to the semiconductor device which has MOS gate.

[0002]

[Description of the Prior Art] With the element which controls a big current with MOS gates, such as power metal-oxide semiconductor field effect transistor and an insulated-gate bipolar transistor (below Insulated gate bipolar transistor IGBT is called), many MOS cells are formed in a front face, and a current is passed to lengthwise. Cross-section structure is shown in drawing 1, using IGBT as an example. p+ It is n on a layer. - A layer is formed and it is n. - Many p layers are formed from the layer front face. In the interior of p layer, it is n+. The layer is formed. Moreover, n+ A layer, p layers, n - Over a layer, a gate electrode is prepared on a front face at a gate oxide film, and is prepared on it at a pan, and MOS gate is constituted. The gate electrode is insulated with the emitter electrode which is covered by the insulator layer and is wearing a front face. An emitter electrode is p layers and n+. The ohmic contact is carried out at the layer. Moreover, in an opposite side (rear face), it is p+. A layer and a rear-face electrode carry out an ohmic contact, and are a collector electrode.

[0003] With the element of the above-mentioned structure, although it was the technique of preparing and carrying out wirebonding of the putt at the place in which MOS gate is not established conventionally, in order to increase flow area, generally the technique of carrying out direct wirebonding to an emitter electrode uses.

[0004]

[Problem(s) to be Solved by the Invention] Conventionally, the aluminum silicon alloy has been used as an emitter electrode. Since silicon is spread to aluminum with pure aluminum and pn junction is destroyed, this is for preventing it. In power metal-oxide semiconductor field effect transistor or IGBT, since a big current flows, a wire uses several 100-micrometer thick thing. In order to ease the impact when carrying out bonding of this wire, it is used by LSI, depends and is used by depositing a thick (3 micrometers or more) aluminum silicon alloy. For this reason, the silicon residue which the silicon in an aluminum silicon alloy gathers during deposition, and is made tends to grow. Since a silicon residue becomes large with deposition, area near a front face becomes large as there is thickly small. For this reason, it becomes the configuration where near the front face sharpened. When the wire was struck on this silicon residue, the force concentrated at the nose of cam of a silicon residue, the crack went into the insulator layer, and there was a problem that an insulation of an emitter electrode and a gate electrode was destroyed. this invention aims at offering the semiconductor device which improved the yield at the time of wirebonding, with the main pressure-proofing yield equivalent to the former maintained.

[0005]

[Means for Solving the Problem] In the semiconductor device with which an emitter electrode is prepared MOS gate and on it, and bonding of the wire is further carried out to the emitter electrode, pure aluminum is prepared in an emitter electrode, and this invention prepares a barrier layer between an emitter electrode and MOS gate, in order to solve the above-mentioned problem.

[0006] A silicon residue can be lost by using pure aluminum. The crack which this generates at the time of wirebonding can be prevented, and the yield at the time of wirebonding can be improved. Furthermore, since it can prevent that silicon is spread to aluminum by the barrier layer, and pn junction destroys, the main pressure-proofing yield equivalent to the former is obtained.

[0007]

[Embodiments of the Invention] An example is explained in detail below using a drawing. Drawing 2 shows the 1st example of this invention. n- Much p layer 2 is formed from the layer front face 1. In the 2 interior of p layer, it is n+. The layer 3 is formed. Moreover, n+ A layer 3, p layer 2, n - Over a layer 1, the gate electrode 11 is formed on a front face at the gate oxide film 10, and is prepared on it at a pan, and MOS gate is constituted. The gate electrode 11 is insulated with the emitter electrode 20 which is covered by the insulator layer 12 and is wearing a front face. The emitter electrode 20 is 2 and n+ p layers. The ohmic contact is carried out at the layer 3. Bonding of the wire 30 is carried out on the emitter electrode 20. Moreover, the barrier layer 21 is formed between the emitter electrode 20 and the insulator layer 12. The emitter electrode 20 is formed of pure aluminum.

[0008] A silicon residue can be lost by using pure aluminum. The crack which this generates at the time of wirebonding can be prevented, and the yield at the time of wirebonding can be improved. Furthermore, since it can prevent that silicon is spread to aluminum by the barrier layer, and pn junction destroys, the main pressure-proofing yield equivalent to the former is obtained.

[0009] Since the contact resistance with silicon tends to get used to small being a thing, that it can be equal to hot heat treatment, and the conventional silicon process as a barrier layer 20, a molybdenum silicide is desirable. By the way, since silicon will be

spread if a barrier layer is not much thin, the main pressure-proofing yield falls. Drawing 3 shows the thickness of a molybdenum silicide, and the relation of the main pressure-proofing yield. The poor main pressure-proofing is [ the thickness of a molybdenum silicide ] 0 by 600A or more. When using a molybdenum silicide as a barrier layer, 600A or more is more nearly required than this.

[0010] Drawing 4 is an example when constructing the semiconductor device of this invention to a module. On the electric insulating plate 50, the collector wiring 51, the emitter wiring 52, and the gate wiring 53 are formed. A chip 60 is formed on the collector wiring 51, and the collector is connected to the collector wiring 51 and drawing through the rear-face electrode which has not appeared. The gate putt 40 is formed in chip 60 front face, further, a protective coat is removed partially and, as for the flow field, the emitter putt 41 is formed. The gate putt 40 and the gate wiring 53 are connected by the gate wire 31, and the emitter putt 41 and the emitter wiring 52 are connected with the emitter wire 32. Since failures would occur frequently by the crack by the silicon residue if bonding of the wire is conventionally carried out by the not much strong force, it attached by the weak force. In the semiconductor device of this invention, when a current is repeated and added to a wire since bonding can be carried out by the force stronger than the former since there is no silicon residue, a life until a wire peels can be prolonged.

[0011] Drawing 5 shows the example of the inverter circuit for motorised constituted using the semiconductor device of this invention. With the notation of a drawing, although the semiconductor device shows only one piece, in order that it may pass a high current, two or more semiconductor devices are connected in parallel. Diode 201 is connected to the semiconductor device 200 at the reverse parallel, a semiconductor device is connected to a two piece serial, and one phase is formed. The output has come out from the middle point where the semiconductor device was connected, and it connects with the motor 206. The semiconductor devices [ by the side of an upper arm / 200a, 200b, 200c, and 200d ] collector is common, and is connected the high potential side of a rectifier circuit. Moreover, the semiconductor devices [ by the side of a lower arm / 200d 200e, and 200f ] emitter is common, and is connected the grounding side of a rectifier circuit. A rectifier circuit 203 changes alternating current 202 into a direct current. A semiconductor device 200 receives this direct current, changes it into an alternating current again, and drives a motor. The up-and-down drive circuit 204,205 tells a driving signal to the gate of a semiconductor device, and makes a semiconductor device turn on and turn off with a predetermined period. By the module incorporating the semiconductor device of this invention, since time until a wire peels becomes long when repeating a current on a wire, the reliability of an inverter can be raised.

[0012]

[Effect of the Invention] A silicon residue can be lost by using pure aluminum. The crack which this generates at the time of wirebonding can be prevented, and the yield at the time of wirebonding can be improved. Furthermore, since it can prevent that silicon is spread to aluminum by the barrier layer, and pn junction destroys, the main pressure-proofing yield equivalent to the former is obtained.

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[Translation done.]

|   | Type | L # | Hits | Search Text   | DBs          |
|---|------|-----|------|---|--------------|
| 1 | IS&R | L1  | 1    | ("4412885").PN.   | USPAT        |
| 2 | IS&R | L2  | 474  | (257/327,328).CCLS.   | USPAT        |
| 3 | BRS  | L3  | 705  | semiconductor and interconnect\$3 same aluminum same titanium adj nitride | USPAT        |
| 4 | BRS  | L4  | 2    | jp-11284176-\$.did.   | JPO; DERWENT |
| 5 | BRS  | L7  | 37   | barrier same molybdenum adj silicide same titanium adj nitride            | USPAT        |